Exhibit K

From: Jeff Bragalone [jbragalone@ShoreChan.com]
Sent: Monday, January 23, 2006 7:55 PM
To: G. Hop Guy; Michael Headley
Cc: Joseph Depumpo
Subject: FW: Documents from Shore Chan LLP

Attachments: Document.pdf


Document.pdf (1 MB)

Hopkins and Michael -

Attached is a copy of a document that we intend to show to Mr. Beasom in preparation for the upcoming depositions.

-- Jeff

SHORE CHAN
BRAGALONE LLP
Attorneys & Counselors at Law

Jeffrey R. Bragalone
325 North Saint Paul St.
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Dallas, Texas 75201
214-593-9125 (Direct)
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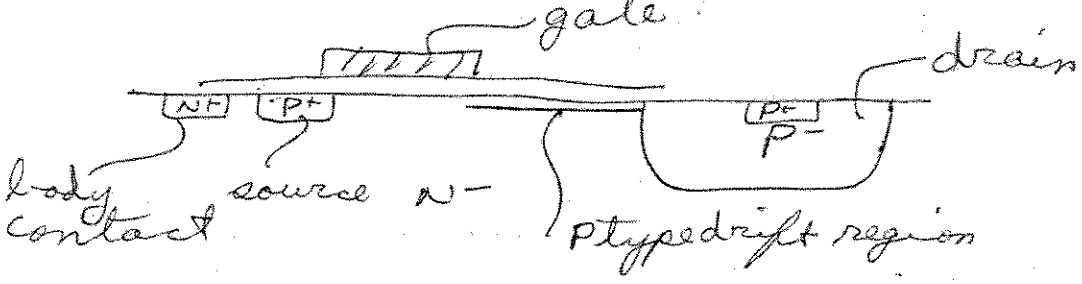
Please open the attached document. This document was digitally sent to you by Shore Chan Bragalone LLP.

4/20/84

lateral drift region MOS with reduced drift region resistance

A known method of fabrication of high voltage MOS devices which have self isolated drains is use of lateral drift region shown below for a PMOS in n substrate.



The high voltage junction is the P^--n-junction. It is connected to the gate by a low concentration P drift region. The drift region acts as a JFET with the substrate as gate. It is designed to totally deplete ~~before~~ at a bias voltage to the n- body less than the breakdown voltage of the P drift to n- junction. The resistance

R.D. Moore 4/25/84
John Porter 4/25/84
James Beason April 20, 1984

4/20/84

of the region is the major term in the on resistance of the device.

This resistance can be reduced by adding an n layer above the P drift region. The n layer acts as a topgate to the PJFET and allows more P charge for a given total depletion voltage thereby allowing one to achieve lower Ron.

The n layer must be designed so that it is totally depleted before n layer to P drain breakdown voltage is reached.

Provision must also be made to insure that the channel is in contact with the P layer either by making the n layer shallower than the depth of the inversion layer or by causing the P layer to come to the surface at the edge of the n layer. The latter can be accomplished

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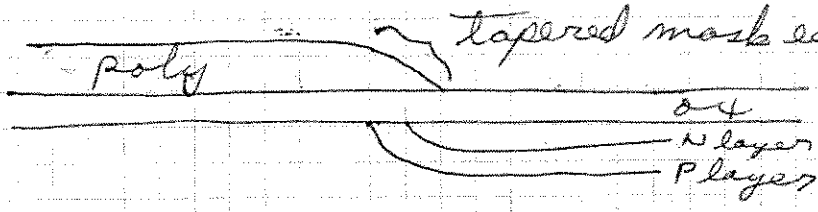
SIGNED R.D. Moore DATE 4/25/84

SIGNED John Pantie DATE 4/25/84

James D Beasom
April 20, 1984

or at least two ways. One is to form the N and P layers by implant with the P implant depth greater. A tapered mask edge will retard both implants such that they curve up to the surface as shown below where the mask is a poly gate.



Another method is to use species with different diffusion coefficients such that the top gate diffuses more slowly and allow the channel layer to diffuse laterally to achieve the required contact.

For proper action, the N layer should be in contact with the N- substrate.

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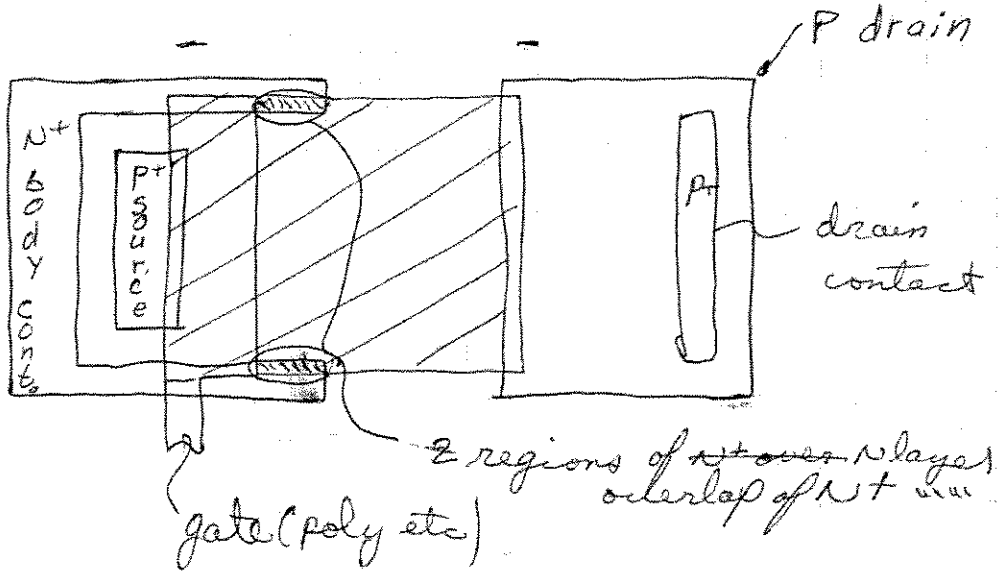
electrically. an easy way to insure this is to have both layers overlap a n diffusion (could be body contact) which is deeper than P layer and has higher concentration than P layer. Such a geometry might look like:



/// = thin ox

The N layer and P drift region can be implanted through thin

RD Moore 4/25/84
poly buffer 4/25/84

James D Beason
April 20, 1984

DATE 4/20/84

oxide as shown above as formed under a thick oxide such as a local oxidation as is often done for drift regions in conventional high voltage structures.

N channels devices can be made in P substrates using the same concepts.

SIGNED RD Moore DATE 4/25/84 James D Beasom

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Exhibit L

CONFIDENTIAL DOCUMENT

Exhibit M

From: Michael Headley
Sent: Tuesday, May 02, 2006 6:06 PM
To: Brian Vanderzanden (bvanderzanden@orrick.com)
Subject: Re: PI-Fairchild: prior art dates

Brian,

I received your letter of today regarding Fairchild's proposal with respect to stipulating to the dates of publication for various prior art references. Again, your letter misrepresents the nature of our discussions with respect to alleged prior art and attempts to divert the parties' attention with a raft of art that will never be addressed at trial. I am writing to correct the record and, I hope, to put the parties on track toward a meaningful discussion of the issue.

First and foremost, your stipulation includes a wide range of art that is not relevant for trial, including art not addressed in Fairchild's experts' reports and art related to positions Fairchild appears to have abandoned. It is clear that Fairchild will not rely on 106 pieces of art at trial; it is equally clear that the parties will be able to stipulate to the dates of publication for many references. To keep the parties from wasting time with unnecessary matters, please let us know what art Fairchild truly intends to rely on at trial, and we will let you know which dates of publication we can accept.

Second, your letter incorrectly suggests that Fairchild sent Power Integrations a stipulation in November, when in fact the first of the various (and increasingly lengthy) versions of Fairchild's proposed prior art stipulation arrived in April. Although I raised problems with the dates for various references Fairchild raised in its expert reports in November with Mr. de Blank, he did not get back to me at that time. Power Integrations cannot be blamed for Fairchild's delay in addressing the issues I raised at that time.

Third, the wording of the stipulation is not acceptable to Power Integrations. If we are to stipulate to the publication dates for various references, we will stipulate that "(reference) was published as of (date)." As phrased, your stipulation suggests additional weight be given to references with respect to section 102.

I look forward to your response.

Sincerely,

Michael R. Headley
Fish & Richardson P.C.
500 Arguello St., Suite 500
Redwood City, CA 94063-1526
(650) 839-5139 (direct)
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Exhibit N

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May 22, 2006

Brian VanderZanden
Orrick, Herrington & Sutcliffe LLP
1000 Marsh Road
Menlo Park, CA 94025

Re: Power Integrations Inc. v. Fairchild Semiconductor Int'l
USDC-D. Del. - C.A. No. 04-1371-JJF

Dear Brian:

I received your letter of last week regarding a stipulation for prior art dates, but Fairchild's proposal again contains the same flaw as the previous draft: the list includes a wide range of material that will not be used at trial. Power Integrations cannot be expected to bear the burden of addressing Fairchild's list of more than 75 references simply because Fairchild is unable (or unwilling) to pare its list to a reasonable size at this point.

Sincerely,

Michael R. Headley

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Date May 22, 2006

To Brian VanderZanden
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From Michael R. Headley

Re Power Integrations, Inc. v. Fairchild Semiconductor International

Number of pages including this page 3

Message